Exercise (SS 2022) Comunication Systems and Protocols

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Task 1: CAN Bus

Since CAN uses CSMA/CR as arbitration scheme every participant compares the actual bus level with the signal transmitted by itself. Because of that it is important for every participant to be able to evaluate the actual state on the bus before begin of a new bit. Here beside the signal runtime on the bus also the required processing time of the participant itself plays a role.

As given in Figure 1.1, this includes the processing time t_{CAN} of the CAN controller, the times t_{Rx} and t_{Tx} which are needed inside the transceiver for reception and transmission as well as the runtime t_{Bus} on the bus.

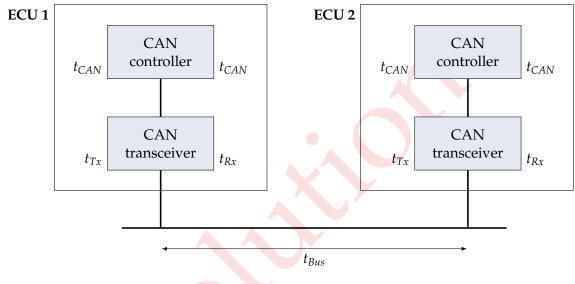


Figure 1.1: CAN bus

1.1 What is the interrelation between the maximum bus length and the bit transmission rate for CAN? Neglect the processing time inside the ECUs for this question

Condition of simultaneity has to be fulfilled. T_{Bit} : Duration for transmission of one bit T_{Prop} : Signal runtime on the bus

Interrelation: $T_{Bit} >> T_{Prop}$

$\Rightarrow \frac{1}{TR} >> \frac{l}{v}$ *TR*Transmission rate, *l* Maximum bus length, *v* Velocity of propagation

1.2 Based on the previous question, specify the maximum bus length for a speed of propagation of $v = 2.3 \cdot 10^8 m/s$ and for the transmission rates of 10kbit/s and 1Mbit/s respectively.

First node to start an arbitration has to wait at least 2 times the duration for propagation of a signal on the bus until it gets a valid signal on the bus:

• One node starts arbitration. After 1x T_{Prop} the signal reaches the node at the end of the bus.

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- Now this node knows that a new arbitration has started and sends out its own ID bit.
- The signals reaches the first node after another T_{Prop} . Now we have a stable value on the bus, $2x T_{Prop}$ after the first node started transmission.

 $\begin{array}{l} T_{Bit} \geq 2 \cdot T_{Prop} \Rightarrow l \leq \frac{v}{2 \cdot TR} \\ \text{For 10kbits/s: } l \leq \frac{2.3 \cdot 10^8 m/s}{2 \cdot 10 k b i t/s} \Rightarrow l \leq 11500m \\ \text{For 1Mbit/s: } \Rightarrow l \leq 115m \end{array}$

1.3 Now also consider the delays inside the ECUs. What is the maximum data transmission rate if the bus length between the two furthest controllers is 300 meters? The detection of the bus state shall be accomplished after 80% of the bit time at latest. (assume: $t_{CAN} = 75nsec$, $t_{Rx} = t_{Tx} = 25nsec$, $v_{Bus} = 0, 2m/nsec$).

Delay inside the participants: $t_{TN} = 2 \cdot t_{CAN} + t_{Tx} + t_{Rx} = 2 \cdot 75ns + 2 \cdot 25ns = 200ns$ Delay on the bus: $t_{Bus} = \frac{l_{Bus}}{v_{Bus}} = \frac{300m}{0.2m/ns} = 1500ns = 1.5\mu s$ Minimum bit duration: $t_{Bit} \ge 2 \cdot (t_{TN} + t_{Bus}) = 2(0.2\mu s + 1.5\mu s) = 3.4\mu s$

The detection of the bus state occurs after 80% of the bit duration. This is to ensure a safety margin of 20%. Now we need to compute the bit duration which has this safety margin.

 $t_{Bit_80} = \frac{t_{Bit}}{0.8}$ Maximum transmission speed when there is the safety margin is: $S = \frac{1}{t_{Bit_80}} = \frac{0.8}{t_{Bit}} = \frac{0.8}{3.4\mu s} = 235Kbit/s$

Task 2: Universal Serial Bus (USB)

2.1 Consider an USB 1.1 device in reset state. Calculate the current on the bus. Neglect the energy needs of the device itself. Use the circuit in Figure 2.1 as orientation. The current flow on the bus is determined by the series connection of R_1 and R_2 :

$$R_{1} + R_{2} = 15k\Omega + 1,5k\Omega = 16.5k\Omega$$
$$I = \frac{U}{R} = \frac{3.3V}{16.5k\Omega} = 200\mu A$$

As a comparison: Maximum current consumption in standby in accordance with the specification: $500\mu A$.

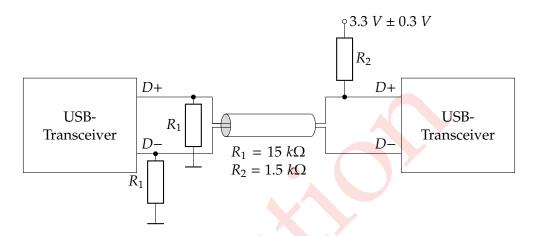


Figure 2.1: Example for resistor configuration at 12Mbit/s

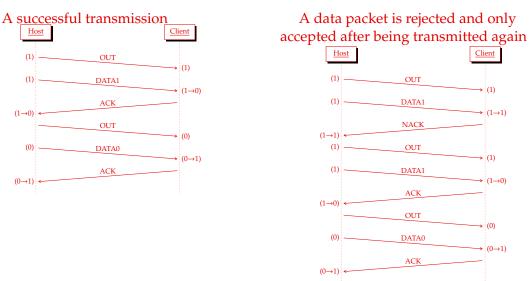
2.2 To reduce the probability of errors during the handshake phase of a transaction, two data PIDs (DATA0 and DATA1) are used. The data PID is changed after every successful transmission. For that reason the sender and the receiver both have a "data toggle sequence bit". At the receiver this only changes if correct data with a correct PID has been accepted. At the sender it changes when a valid ACK-Handshake is received. Both participants of a transmission first have to synchronize their bits during the setup phase of a control transfer (see Figure 2.2, the bracketed values correspond to the value of the "data toggle sequence bits"; at X/Y they are still undefined).

Starting from the state of 2.2, specify the flow charts for the following cases (always consider a transfer from host to device):

- 1. A successful transmission
- 2. A data packet is rejected and only accepted after being transmitted again
- 3. The handshake packet of a transmission has been mutilated. The data is transmitted again and accepted then

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The handshake packet of a transmission has been mutilated. The data is transmitted again and accepted then

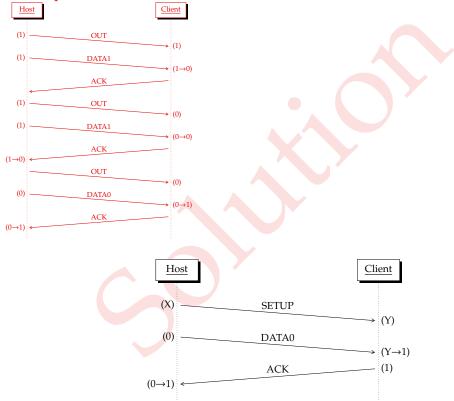


Figure 2.2: Synchronization of the data toggle sequence bits

Task 3: Routing - old exam question

Switching

3.1 Figure 3.1 shows a network topology with equal weights w_n on every link. Give the number of hops of the route from node A to F using *minimal routing*. In addition, describe how the number of hops from A to F could change if weights are differing and non-minimal routing is used.

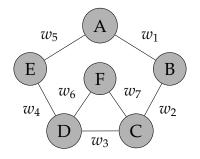


Figure 3.1: A network topology

Hops with minimal routing: 3

If non-minimal routing is used, a route using nodes C and D could become the optimal route with 4 hops.

Correction hints: 1pt for 3 hops, 2pt for explanation (node C/D, 4 hops)

12

ID:

3.2 Figure 3.2 represents a network for which an optimal routing has to be found. The weights represent an abstract metric for traffic present at each connection. With node **A** as the starting point, calculate the paths with the lowest total traffic in the network by using Dijkstra's algorithm. Fill in Table 3.1 with the order in which nodes are visited in each step and the shortest paths after visiting the corresponding node. Make sure to fill all fields of Table 3.1.

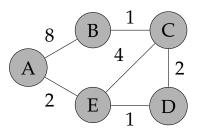


Figure 3.2: Given network topology

	step 0		step 1		step 2		step 3		step 4		step 5	
node	Α		А		Е		D		С		В	
vertex	dist.	pred.	dist.	pred.	dist.	pred.	dist.	pred.	dist.	pred.	dist.	pred.
А	0	A	0	A	0	A	0	A	0	A	0	A
В	∞	-	8	Α	8	Α	8	Α	6	С	6	С
C	∞	-	∞	-	6	Е	5	D	5	D	5	D
D	∞	-	∞	-	3	Е	3	Е	3	Е	3	Е
Е	∞	-	2	A	2	А	2	А	2	А	2	А

Table 3.1: Dijkstra's algorithm

Correction hints: 2 Points steps 2, 3 and 4 each; 1 Point for steps 1 & 5 each; 1 Point for visited nodes